Remarks

Claims 1-33 are pending in the application. Independent claims 1 and 18 have been amended and claims 2 and 19 have been canceled herein. Favorable reconsideration of the application, as amended, is respectfully requested.

Claim Rejections - 35 USC § 102 and § 103

Claims 1-2, 5, 9-10, 13, 17-19, 22, 25-26, 29 and 32-33 stand rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 6,153,467 to *Wu*. Claims 3-4, 6-8, 11-13, 15, 20, 23-24, 27-8 and 30-31 stand rejected under 35 USC §103(a) as being unpatentable over *Wu*. Withdrawal of the rejection is requested for at least the following reasons.

Independent claims 1 and 18 have been amended herein and now recite that the source and drain regions extend substantially to the bottom of the trench. This is advantageous in that the channel region 52, which is below the trench, can extend beyond the confines of the respective source 54 and drain 56 regions, thereby increasing channel length while minimizing a curvature of the channel region at an apex of the trench. Support for this amendment can be found, for example, in Figs 1A and 3G.

Wu discloses a flash EEPROM that includes a conductive layer 170 that operates as the bit line for the flash EEPROM.[1] As is conventional, the bit line is connected to the source and drain regions of the memory cell, which is above the conductive layer 170 or "bit line".[2] As can be seen in Figs. 3-8 of *Wu*, the conductive layer 170 is above the bottom of the trench 150. Additionally, *Wu* expressly teaches that the trench is formed by dry etching to remove the oxide layer, pad oxide layer and *conductive layer* (i.e., the bit line) so as to form a recess in the silicon substrate.[3] Thus, the bottom of the trench is below the bit line and, therefore, *Wu* does not teach that the source and drain regions extend substantially to the bottom of the trench, as recited in amended claims 1 and 18.

Further, it would not have been obvious to modify *Wu* to reduce the trench depth so as to be substantially the same as the source/drain depth (or extend the source and

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[1] See Fig. 9 of *Wu*.

[2] The region below the conductive layer 170 or "bit line" is the silicon substrate 100, see, e.g., Fig. 8 of *Wu*.

[3] Column 3, lines 40-46 of *Wu*.

drain depth to be substantially the same as the trench depth). As noted above, *Wu* expressly teaches that the trenches are formed by dry etching to remove the oxide layer, pad oxide layer and *conductive layer* (i.e., the bit line) so as to form a recess in the silicon substrate. Reducing the depth of the trench to be equal to the source and drain regions would be contrary to the express teachings of *Wu*. Further, *Wu* does not indicate that any benefit can be expected by extending the source/drain regions to substantially the same depth as the trench.

Although not discussed by the Examiner, the remaining art to *Wu* (U.S. 6,137,132), *Lee et al.* (U.S. 5,773,343), *Liu* (U.S. 6,147,377) and *Forbes* (U.S. 6,853,587) have not been found to teach that the source and drain regions extend to substantially the bottom of the trench.

Accordingly, withdrawal of the rejection of claims 1 and 18 is respectfully requested.

Claims 2-17 and 19-33 directly or indirectly depend from claims 1 or 18 and, therefore, can be distinguished from the cited art for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 2-17 and 19-33 is respectfully requested.

Conclusion

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

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